

# Tackling Advanced Technology Boards: Combining X-Ray and ICT

By Ed Crane, Ed Kinney and Bill Jeffrey

A combination of in-circuit test and automated x-ray inspection may help you lower overall costs, improve product quality, and speed time to market.

**D**eveloping a robust test strategy for the manufacture of large, high-density printed circuit board assemblies (PCBAs) to assure design compliance and functionality is important. In addition to the building and testing of these complex assemblies, the money invested in electronic parts alone can be substantial—dollar value may reach \$25,000 when a unit reaches the final testing operation. Because of this high cost, detecting and repairing assembly problems are even more important procedures now than they were in the past. Today’s more complex assemblies are approximately 18 in.<sup>2</sup> with 18 layers; have more than 2,900 components top and bottom; contain more than 6,000 circuit nodes; and have more than 20,000 solder joints requiring test.

At Lucent Technology’s manufacturing facility (N. Andover, MA), state-of-the-art PCBAs and complete transmission systems are manufactured and tested. Assemblies

that exceed a 5,000-node count are a concern to us as they approach the resource limit of our current in-circuit test (ICT) equipment (Figure 1). We presently manufacture approximately 800 different PCBAs or “codes.” Of the 800 codes, approximately 20 are in the 5,000 to 6,000 node range. That number, however, is growing quickly.

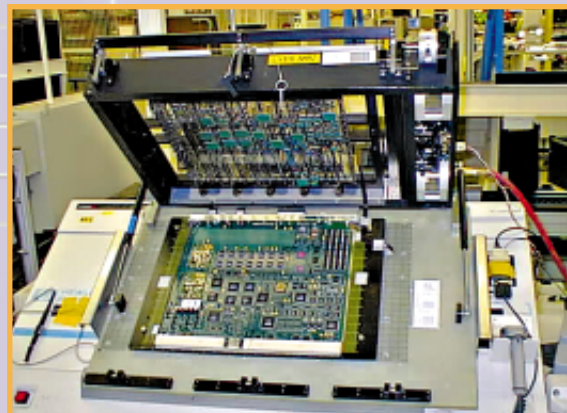
New development projects are requiring PCBAs that are more complex, physically larger and more tightly packaged. These requirements challenge our ability to build and test the units. Furthermore, this trend of larger boards with smaller components and higher node counts will probably continue. For example, one design currently on the drawing board has approximately 11,600 nodes, over 5,100 components and over 37,800 solder joints that require testing or verification. This unit also has ball grid arrays (BGAs) on both the top- and bottom-side of the board, with the BGAs located back to back. Testing a board of this size and complexity using conventional bed-of-nails, in-circuit test- (ICT) only methods is impossible.

The reality of ever increasing PCBA complexity and density in manufacturing processes, especially testing, is not a new

concern. Realizing that increasing the number of nails built into ICT test fixtures was not the direction to take, we began to look at alternative circuit verification methods. Looking at the numbers in terms of missed contacts per million probe attempts, we found that, at 5,000 nodes, a number of faults detected (less than 31) could be attributed to missed probe pad contacts rather than actual fabrication errors (Table 1). Therefore, we worked to drive the nail count down, not up. However, the quality of our manufacturing processes must still be evaluated over the entire PCBA. We determined that using a combination of conventional ICT (Sidebar A) and x-ray laminography (Sidebar B) is a viable solution.

## Test Strategy

Our overall test strategy relies heavily on boundary scan, which provides a partial solution. Many components cannot be verified at ICT, and many complex ASICs have redundant power and ground pins that must be verified. Opens on these pins may cause long-term reliability problems. The test strategy we have adopted is verifying the acceptability of each solder joint on the



**FIGURE 1:** This complex in-circuit test fixture is shown with the over-clamp assembly raised. The board under test can be seen in the middle of the fixture. A fixture such as this one can weigh as much as 200 pounds and is unique to each board design.

# Test Strategy

entire board using an automated x-ray laminography inspection system. In the strategy, production PCBAs are routed through the x-ray system. The defective boards are routed to our repair station for corrective action and re-inspection. PCBAs that pass inspection are moved to an in-circuit board test system for further testing. This strategy is in its final phase of implementation for advanced technology assemblies currently in production. PCBAs in the

model or development/prototype phase of design realization are x-rayed for solder joint integrity only, as test fixtures and/or test programs for the in-circuit tester are generally not available at that time.

Using production x-ray inspection for model evaluation has allowed diagnostic technicians to rule out solder joint-related problems, such as opens, shorts, missing components, insufficient solder and some polarity orientation issues. This new

process has saved both time and money. Currently, fabrication test runs for development models tend to be approximately the same size as production runs. Model runs may be in the 150-unit range, and production runs of high-end PCBAs are in the 200-unit range.

Our PCBAs are built using automatic pick-and-place machines, manual connector placement, and manual faceplate assembly. Testing completed assemblies using

## How In-Circuit Test Works

In-circuit testing (ICT) is the process of verifying the electrical integrity of a circuit subassembly by probing test points scattered across the board's surface. For automated testing, the probes are spring-loaded "pins" mounted on a thick phenolic plate and wired separately to a switching matrix. The switching matrix is an array of relays that connects the appropriate pins to the current sources and voltage-measuring instruments required at each step in the test procedure.

The phenolic plate carrying hundreds to thousands of spring-loaded pins resembles a bed of nails, and test engineers have adopted the term "bed-of-nails fixture" for the plate. Each nail is positioned so that, when the board is placed on the fixture and pulled down by a vacuum apparatus, the nail contacts its target test point without shorting to neighboring circuit structures.

ICT can verify the existence of conducting paths, rule out the possibility of short circuits, measure individual resistors and inductors, and detect the presence and orientation of diodes, transistors and integrated circuits. ICT typically cannot determine the polarity of polarized capacitors or identify missing bypass capacitors. However, it can detect shorted capacitors and open inductors.

Basic ICT has been enhanced over the years with techniques that overcome its limitations in the face of advancing technology. For example, when integrated circuits became so large that providing probe targets for significant percentages of the circuit was impossible, ASIC engineers developed the boundary scan technique. Boundary scan provides an industry-standard method to verify device interconnects where probe access is not present. Additional circuits designed into an IC allow the device to communicate with surrounding devices in a simple fashion and present the results of the test in an easily detectable format.

Another vectorless technique applies an AC signal through the bed of nails to the device under test. A sensor plate pressed against the top surface of the device under test forms a capacitor with the device's lead frame and couples a signal to the sensor plate. The absence of the coupled signal indicates an open solder joint.

The labor needed to devise a test program for a large, complex board is monumental. Luckily, automated test program generation (ATPG) software can automatically design the required fixture and test procedure based on the PCBA's CAD data and libraries for specifications of the components placed on the board. While these techniques help reduce the program generation time, the prove-in of the high node count test program and fixture is still a time-consuming and technically challenging endeavor.

## How X-Ray Laminography Works

PCBA manufacturing is essentially a matter of soldering prefabricated components onto a prefabricated printed wiring board. Theoretically, as long as the correct components are placed in the correct locations in the correct orientations and are electrically connected with good solder joints, the PCBA will operate as designed. Therefore, the test problem for a PCBA manufacturer boils down to ensuring the quality of the solder joints—a structural inspection.

When solder joints are hidden under large integrated circuit (IC) packages, inspecting them requires x-rays. X-rays can penetrate IC packages but are absorbed by the much denser lead-based solder, leaving their images as shadows. A simple x-ray shadowgraph, however, becomes confused by the metallic conductors in overlying ICs' internal structures and underlying layers of multilayer circuit boards. The situation becomes even worse when PCBAs have circuitry on both sides.

X-ray laminography, or 3-D x-ray, is a technique for isolating horizontal planes in PCBAs so that they can be inspected separately. As with a shadowgraph, the technique starts with a collimated source of x-rays and an imaging detector array. Unlike the shadowgraph technique, the laminography x-ray beam passes through the board at an angle. The detector is directly under the board structures in the field of view (FOV) but is offset to intercept the x-ray beam coming through at an angle.

During the course of imaging, both the detector and source rotate around an axis passing through the FOV. Image smearing causes structures in the imaging plane to appear stationary while objects above and below the plane move rapidly in a circular motion, appearing unfocused and rapidly disappearing from view. This phenomenon is similar to looking "through" the rotating propeller of an airplane.

Based on details of the resulting image, a computer algorithm can determine the exact shape of the solder joint fillet and detect voids within the joint. It can also compute the volume of solder. These measures indicate the solder joint's quality. The technique can also detect solder bridges that may result in short circuits.

# Test Strategy

	5.5	5.6	5.7	5.8	5.9	6	<=Sigma
pins	31.7	20.6	13.3	8.5	5.4	3.4	<=PPM rate
0	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	
500	1.6%	1.0%	0.7%	0.4%	0.3%	0.2%	
1000	3.2%	2.1%	1.3%	0.9%	0.5%	0.3%	
1500	4.8%	3.1%	2.0%	1.3%	0.8%	0.5%	
2000	6.3%	4.1%	2.7%	1.7%	1.1%	0.7%	
2500	7.9%	5.2%	3.3%	2.1%	1.4%	0.9%	
3000	9.5%	6.2%	4.0%	2.6%	1.6%	1.0%	
3500	11.1%	7.2%	4.7%	3.0%	1.9%	1.2%	
4000	12.7%	8.2%	5.3%	3.4%	2.2%	1.4%	
4500	14.3%	9.3%	6.0%	3.8%	2.4%	1.5%	
5000	15.9%	10.3%	6.7%	4.3%	2.7%	1.7%	
5500	17.4%	11.3%	7.3%	4.7%	3.0%	1.9%	
6000	19.0%	12.4%	8.0%	5.1%	3.2%	2.0%	
6500	20.6%	13.4%	8.6%	5.5%	3.5%	2.2%	
7000	22.2%	14.4%	9.3%	6.0%	3.8%	2.4%	

FORMULA: (100 boards X PPM rate X #of Pins)/(1M \*100) = % of 100 boards that will have one false call.

**TABLE 1:** Achieving acceptable false-negative rates requires probe-contact quality that cannot be maintained when fixtures have several thousand pins.

both x-ray and ICT technologies verifies our assembly processes. The test program ensures that the correct parts have been placed on the boards in the correct locations and orientation, and x-ray determines that all solder joints have been properly made. At this point functionality is not determined. The business units receiving the boards elect whether or not to do a board-level functional test. That decision is made on an individual board basis. Next, PCBAs are installed into shelves, shelves are put into frames and frames are connected to frames. Finally, the whole system is tested functionally. All of the assemblies receive a functional test during final system test. After favorable testing, the system is shipped to the end customer.

## X-Ray/ICT Interaction

PCBAs that exceed the 5,200 net limit of the ICT machines are impossible to test using conventional ICT with bed-of-nails fixturing. Furthermore, none of our assemblies may be tested fully on the in-circuit testers anyway. Typically, 10 to 15 percent of the board's core circuitry cannot be tested. For example, bypass capacitors and power and ground pins of ASIC devices are invisible to DC-level measurements. Because these nodes cannot be tested using normal ICT, we validate them using our x-ray laminographic process. Before use of the x-ray, typical coverage on large boards was between 60 and 70 percent. Including

x-ray in the test strategy provides over 99 percent test coverage on the boards. For components whose solder joint integrity is being confirmed by the x-ray system, an assumption has been made that our up-front processes have been followed to assure that correct components have been placed on the board.

Additionally, we have to verify that the board is structurally connected—all the solder joints have been correctly made and no internal shorts or opens exist. That verification is performed with x-ray inspection.

For ICT on ASICs, boundary scan is used quite extensively, which allows our testers to quickly read the ID registers of the ASICs. If successful, boundary scan indicates that the ASIC is in place and oriented properly. Previously verifying the structural integrity of the solder joints reduces the number of nodes that the bed-of-nails fixture needs to contact. The ICT will not be required to toggle every ASIC pin to determine whether it is open or not.

By using the specific x-ray laminography inspection system, we have been able to decrease the required node count by 40 percent on average. The reduced ICT node count lowers fixture complexity and cost and also results in fewer false calls, which allows boards to move through our rework and manufacturing process faster. Using x-ray has also increased first-pass yield at ICT by 20 percent. Using the x-ray/ICT

combined strategy has lowered overall cost, improved the reliability and quality of outgoing products, and allowed quicker shipment of products.

## X-Ray/ICT Strategy's Future

Presently, only a small percentage of the boards on our production lines exceeds the ICT limit of 5,200 nodes. We expect that percentage to grow steadily in the near future.

Also, as we gain experience and increase x-ray capacity, we may apply our new strategy to nodal count PCBAs as low as 2,500 nodes. Because yield issues currently exist with boards in the 4,000-to-5,000-node range due to probe contact problems rather than actual assembly problems, we expect to see an improvement using the combined x-ray/ICT strategy.

In the early 1990s we decided to standardize the ICT system choices our test engineers could make to three configurations, rather than having an open-ended strategy. We decided on 1,900-node; 3,900-node; and 5,200-node configurations. Currently, we have upgraded almost every test set to either 3,900- or 5,200-node machines with a tendency toward 5,200-node systems.

Further use of combined x-ray laminography and ICT technology is ideal because each technology compensates for the other's weakness. X-ray mainly focuses on solder joint quality. It can also verify that a compo-

# Test Strategy

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**FIGURE 2:** The HP 5DX

ment is present at a solder site but generally cannot determine that the component is correct, in the correct orientation, or of the correct value. On the other hand, ICT can determine component orientation and values but cannot determine if a solder joint is acceptable, especially under large surface-mount component packages.

In the near future, we hope to make test strategy decisions on new circuit designs immediately after schematic capture. At that point on high node count schematics, we would like to decide which nodes should be tested via an ICT machine and which nodes should be tested via an x-ray machine. Currently, we cannot make that decision until a design is much further along in the development process.

Ideally, software could generate tests for both x-ray and in-circuit technologies, and the ICT test program should be significantly smaller. The test strategy information could be passed along to the computer-aided

design (CAD) layout system and would contain a smaller number of nodes requiring test pad features. An added benefit in the reduction of test pads is that the board real estate savings should make the layout task somewhat easier. Bed-of-nails fixturing would also be simplified with the reduction of contact probes; the potential for nails making poor contact with their targets will also be reduced. In short, better fault coverage could be achieved with less complex programs and less complex fixturing.

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(Figure 2 did not appear in the original CIRCUITS ASSEMBLY article)

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